In the Claims:

1 - 21. (Canceled)

22. (New) A method for manufacturing a thin film transistor array panel used for a liquid crystal display, comprising:

forming a gate line and a gate electrode on a substrate;

forming an insulating layer on the gate line and on the gate electrode;

forming a semiconductor layer on the insulating layer;

forming a data line, a source electrode and a drain electrode on the substrate;

forming a passivation film on the semiconductor layer, the data line, the source electrode and the drain electrode, the passivation film exposing a portion of the drain electrode and a portion of the semiconductor layer;

removing the exposed portion of the semiconductor layer; and

forming a pixel electrode that contacts the exposed portion of the drain electrode.

23 (New) The method of claim 22, wherein the passivation film comprises opaque material.

24. (New) The method of claim 22, wherein a portion of the passivation film is located on the gate line and the gate electrode.

25. (New) The method of claim 24, wherein the removal of the exposed portion of the semiconductor layer exposes a portion of the insulating layer, and

further comprising:

removing the exposed portion of the insulating layer.

26. (New) The method of claim 25, further comprising:

forming a connection portion that overlaps a part of the gate line on the insulating layer.

27. (New) The method of claim 26, wherein a part of the connection portion is exposed outside the passivation film and is connected to the pixel electrode.

28. (New) A method for manufacturing a thin film transistor array panel used for a liquid crystal display, comprising:

depositing a first conductive layer on a substrate;

patterning the first conductive layer to form a gate line and a gate electrode;

depositing an insulating layer on the gate line and on the gate electrode,

depositing a semiconductor layer on the insulating layer;

depositing a second conductive layer on the semiconductor layer;

patterning the second conductive layer to form a data line, a source electrode, and a drain electrode;

depositing a passivation layer on the semiconductor layer, the drain electrode, the source electrode and the data line;

patterning the passivation layer to expose a portion of the semiconductor layer, a portion of the gate line, a portion of the data line, and a portion of the drain electrode;

removing the exposed portion of the semiconductor layer to expose a portion of the insulating layer;

removing the exposed portion of the insulating layer; and

forming a pixel electrode that contacts the exposed portion of the drain electrode.

29. (New) The method of claim 28, further comprising:

forming transparent conductive pads that cover the exposed portions of the gate line and the data line, respectively.

30. (New) The method of claim 28, wherein the first conductive layer comprises

an upper layer and a lower layer of different materials.

31. (New) The method of claim 30, wherein the lower layer comprises Al or an Al alloy, and the upper layer comprises Mo.

32. (New) The method of claim 30, wherein the lower layer comprises Cr, and the upper layer comprises Al or an Al alloy.

33. (New) The method of claim 32, further comprising:

removing the exposed portion of the upper layer.

34. (New) The method of claim 33, wherein the patterning of the second conductive layer exposes a portion of the n+ amorphous silicon layer, and

further comprising:

removing the exposed portion of the n+ amorphous silicon layer after patterning then second conductive layer.